Requested Patent: JP6290233A

Title: LAYOUT VERIFYING DEVICE ;

Abstracted Patent: JP6290233 ;

Publication Date: 1994-10-18 ;

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Application Number: JP19930076839 19930402 ;

Priority Number(s): ;

IPC Classification: G06F15/60 ;

Equivalents: ;

ABSTRACT:

PURPOSE:To automatically check the sizes of respective parts according to individual verification rules and perform efficient layout verification by grouping elements which relate to conditions to be verified by restricted rules and performing size verification by using rule files which are different, group by group.

CONSTITUTION:Element recognition is performed (12) by using inputted layout pattern data 11 and a net list is extracted (13). A maximum drain current is extracted (15) from respective FET parameters of the extracted net list. Minimum line width which satisfies a prescribed current density is found as to lines connected to the drain sides of respective FETs and width found so that an error is generated when the width is smaller than the minimum line width, is written (19) in a DRC rule file. Then a line through which a drain current flows is extracted (19). Lines through which the same drain current flow are put in the same group and a layer figure for DRC in the same shape is added (20) to layout patterns in the same group. Lastly, a check is executed and errors are displayed.